We claim:

1. A method for fabricating a semiconductor device having a plurality of chips including a device chip and a components chip having passive components fabricated thereon, the method comprising the steps of:

providing a plurality of studs with a stud on a first surface of each of the chips;

providing a plate transparent to ablating radiation;

forming a first layer on the plate, the first layer including conducting pads on a first surface of the first layer opposite the plate;

forming a second layer on the first surface of the first layer, where the plate, the first layer and the second layer form an alignment structure;

forming vias in the second layer to expose the conducting pads;

aligning the studs to the vias;

attaching the chips to the alignment structure, so that the first surface of each chip contacts the second layer and the studs make electrical contact with the conducting pads;

attaching a support to the chips; and

ablating an interface between the first layer and the plate using ablating radiation transmitted through the plate, thereby detaching the plate.

2. A method according to claim 1, wherein said step of forming the first layer further comprises providing electrical wiring for interconnecting the chips, the electrical wiring being provided in the first layer connecting to the conducting pad.

3. A method according to claim 1, wherein said step of attaching a support to the chips further comprises the steps of:

providing a support connection stud on the support;

forming a layer including a support conducting pad on a second surface of the chips opposite the first surface thereof;

forming a support connection via in said layer to expose the support conducting pad;

aligning the support connection stud to the support connection via; and

causing the support connection stud to bond to the support conducting pad, thereby bonding the support to the chips.

4. A method according to claim 3, wherein said step of providing a support connection stud further comprises providing solder material on said stud, so that a solder connection between the support connection stud and the support conducting pad is formed in said step of causing the support connection stud to bond to the support conducting pad.

5. A method according to claim 1, wherein said detaching of the plate exposes a second surface of the first layer opposite the first surface thereof, and further comprising the step of forming a connection pad on the second surface of the first layer.

6. A method according to claim 2, wherein said plurality of chips includes a plurality of device chips, and the components chip has a size according to a placement pattern of the device chips.

7. A method according to claim 6, wherein said detaching of the plate exposes a second surface of the first layer opposite the first surface thereof, and further comprising the step of forming a plurality of C4 pads on the second surface of the first layer, the C4 pads making electrical connection with the chips through the wiring in the first layer, the studs and the conducting pads.

8. A method according to claim 6, wherein said detaching of the plate exposes a second surface of the first layer opposite the first surface thereof, and further comprising the step of forming one of (a) a plurality of interconnect studs on the second surface of the first layer and (b) a plurality of interconnect vias on the second surface of the first layer, for making electrical connection with the chips through the wiring in the first layer, the studs and the conducting pads.

9. A method for fabricating a semiconductor device having a plurality of chips including a device chip and a components chip having passive components fabricated thereon, the method comprising the steps of:

providing a plate transparent to ablating radiation;

forming a first layer on the plate;

providing studs on a first surface of the first layer opposite the plate, where the plate, the first layer and the studs form an alignment structure;

forming a second layer including conducting pads on a first surface of each of the chips, a conducting pad contacting each chip;

forming vias in the second layer to expose the conducting pads;

aligning the studs to the vias;

attaching the chips to the alignment structure, so that the first layer contacts the second layer and the studs make

electrical contact with the conducting pads;

attaching a support to the chips; and

ablating an interface between the first layer and the plate using ablating radiation transmitted through the plate, thereby detaching the plate.

10. A method according to claim 9, wherein said step of forming the first layer further comprises providing electrical wiring for interconnecting the chips, the electrical wiring being provided in the first layer connecting to the stud.

11. A method according to claim 9, wherein said step of attaching a support to the chips further comprises the steps of:

providing a support connection stud on the support;

forming a layer including a support conducting pad on a second surface of the chips opposite the first surface thereof;

forming a support connection via in said layer to expose the support conducting pad;

aligning the support connection stud to the support connection via; and

causing the support connection stud to bond to the support conducting pad, thereby bonding the support to the chips.

12. A method according to claim 11, wherein said step of providing a support connection stud further comprises providing an alloy material on said stud, so that a metallic connection between the support connection stud and the support conducting pad is formed in said step of causing the support connection stud to bond to the support conducting pad.

13. A method according to claim 9, wherein said detaching of the plate exposes a second surface of the first layer opposite the first surface thereof, and further comprising the step of forming a connection pad on the second surface of the first layer.

14. A method according to claim 9, wherein said plurality of chips includes a plurality of device chips, and the components chip has a size according to a placement pattern of the device chips.

15. A method according to claim 14, wherein said detaching of the plate exposes a second surface of the first layer opposite the first surface thereof, and further comprising the step of forming a plurality of C4 pads on the second surface of the first layer, the C4 pads making electrical connection with the chips through the wiring in the first layer, the studs and the conducting pads.

16. A method according to claim 14, wherein said detaching of the plate exposes a second surface of the first layer opposite the first surface thereof, and further comprising the step of forming one of (a) a plurality of interconnect studs on the second surface of the first layer and (b) a plurality of interconnect vias on the second surface of the first layer, for making electrical connection with the chips through the wiring in the first layer, the studs and the conducting pads.

17. A semiconductor device including a plurality of chips, the chips having front surfaces and back surfaces, the device comprising:

a support attached to the chips on the back surfaces thereof;

a first layer disposed on the front surfaces of the chips and having a plurality of vias formed therein and conducting pads in registration with the vias;

a plurality of studs corresponding to the vias and disposed therein; and

a second layer attached to the first layer on a surface of the first layer opposite the front surfaces of the chips, the second layer being aligned to the first layer by the studs in the vias, the second layer including electrical wiring connecting to the chips through the studs and the conducting pads,

wherein said plurality of chips includes chips with active devices and a chip without active devices.

18. A semiconductor device according to claim 17, further comprising an attachment layer between the support and the chips, wherein the attachment layer has a plurality of support connection vias formed therein, support connection pads in registration with the support connection vias, and a plurality of support connection studs disposed in the support connection vias and connected to the support connection pads.

19. A semiconductor device according to claim 17, wherein the chip without active devices has passive components fabricated thereon.

20. A semiconductor device according to claim 17, wherein the chip without active devices has a size according to a placement pattern of the chips with active devices.